Build your own VTA design with Chisel

Luis Vega
VTA-generator vision
VTA-generator vision

- Today
- Tomorrow
VTA-generator vision

- Today
  - Edge Xilinx FPGAs

- Tomorrow
  - Edge/cloud FPGAs, ASICs
VTA-generator vision

• Today
  • Edge Xilinx FPGAs
  • “Off-the-menu” selection

• Tomorrow
  • Edge/cloud FPGAs, ASICs
  • “Build your own” customization
VTA-generator vision

• Today
  • Edge Xilinx FPGAs
  • “Off-the-menu” selection
  • Inference

• Tomorrow
  • Edge/cloud FPGAs, ASICs
  • “Build your own” customization
  • Inference and Training
VTA-generator vision

• Today
  • Edge Xilinx FPGAs
  • “Off-the-menu” selection
  • Inference
  • Dense workloads

• Tomorrow
  • Edge/cloud FPGAs, ASICs
  • “Build your own” customization
  • Inference and Training
  • Dense + sparse workloads
VTA-generator vision

- **Crust**: Xilinx, Intel, ASICS
- **Size**: Edge, Cloud
- **Toppings**: Datatypes, compression
- **Shape**: SIMD, Systolic
Chisel enables hardware generators

- Chisel is a Hardware Construction Language (HCL) based on Scala, with the following features:
  - Efficient (easy to generate high-performance hardware)
  - Extensible (easy to parametrize)
  - Portable (easy to target)
  - Maintainable (easy to modify)
Chisel success stories

- ASICs
  - Just Berkeley alone has taped-out 17 chips w/ Chisel (2011-2018) [1]

- FPGAs

[1] Bachrach, J. Keynote Chisel Community Conference 2018
Timeline

• Started on Sept. 2018

• RTL Simulation (Verilator) - Q4 2018

• FPGA prototype - Q1 2019